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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,280	07/29/2003	Jae-Sun Yun	5649-1129	5702

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EXAMINER	
LE, THAO P	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,280	YUN ET AL.	
	Examiner	Art Unit	
	Thao P. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/29/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledge is made of applicants' claim for foreign priority base on an application 10-2002-0054460 filed in Korean on 09/10/02.

Election/Restriction

2. Examiner confirms that Applicants elected to prosecute Claims 12-35 and have canceled Claims 1-11 without prejudice.

Claim Rejections

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 12-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Applicant Admitted Prior Art (AAPA).

Regarding claim 12, AAPA discloses the method of forming a transistor of a non-volatile memory device comprising (See Fig. 2 and Pages 1-2):

. forming a gate pattern on a substrate, the gate pattern including a gate oxide layer 12, a floating gate 14, an inter-gate dielectric pattern 21, and a control gate 22 which are stacked in the order named;

. forming a diffusion barrier layer 30 on an entire surface of the substrate and gate pattern;

. forming a thermal oxidation layer from the oxide layer beneath the floating gate and on the floating gate between the oxygen diffusion barrier layer and the floating gate. It is inherent that when a thermal oxidation process is performed on the oxide layer beneath the floating gate and on the floating gate between the oxygen diffusion barrier layer, curved sides are formed at the two ends of floating gate (Fig. 1) and so a curved side wall portion of the floating gate.

Regarding claims 13-17, AAPA discloses the method of claim 12 and further discloses the steps of forming an insulating layer on the floating gate, heating the insulating layer and the oxide layer in oxygen atmosphere, forming an inter-grate oxide layer on the floating 21, forming silicon nitride layer on the inter-gate oxide layer, forming control gate 22 on the inter-gate layer (Figs. 1-2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art.

Regarding claims 18-24, AAPA fails to disclose the limitations of claims 18-24 such as the a lower portion of the curved side wall portion curves away from the side wall of the gate structure or a length of the lower curved side wall is greater or less than a length of the upper curved side wall. However, these selection of such parameters such as energy, concentration, temperature, time, molar fraction, depth, thickness, direction etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in energy, concentration, temperature, time, molar fraction, depth, thickness, direction etc., or in conbination of the parameters would be an unpatentable

modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

Claims 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art, in view of Tseng et al., U.S. Pub No. 2003/0181053.

Regarding claim 25, AAPA discloses the method of forming a transistor of a non-volatile memory device comprising (See Fig. 2 and Pages 1-2):

. forming a gate pattern on a substrate, the gate pattern including a gate oxide layer 12, a floating gate 14, an inter-gate dielectric pattern 21, and a control gate 22 which are stacked in the order named;

. forming a diffusion barrier layer 30 on an entire surface of the substrate and gate pattern;

. thermally oxidizing the substrate including the diffusion barrier spacer.

It is inherent that when a thermal oxidation process is performed on the oxide layer beneath the floating gate and on the floating gate between the oxygen diffusion barrier layer, curved sides are formed at the two ends of floating gate (Fig. 1) and so a curved side wall portion of the floating gate.

Still regarding claim 25, AAPA fails to disclose the step of etching the diffusion barrier layer to form a diffusion barrier spacer over a lateral side of the gate pattern. Tseng et al. discloses the method of forming a transistor of a non-volatile memory device comprising the step of etching the diffusion barrier layer 520 to form a diffusion barrier spacer over a lateral side of the gate pattern (Fig. 5). It would have been obvious to one having ordinary skill in the art at the time the invention was made to etch the diffusion barrier layer as disclosed in Tseng et al. because the diffusion barrier is etched to expose surface of the substrate for oxygen atoms diffusion and reaction of oxygen atoms with oxygen layer that lied under the gate pattern to form thermal oxidation laye, and for later formation of light doped regions and source/drain regions.

Regarding claims 26-27, AAPA discloses the inter-gate dielectric pattern is made of silicon oxide, silicon nitride, and silicon oxide and the formation of gate pattern comprising forming a device isolation layer, forming gate oxide layer, forming lower

conductive pattern on the gate oxide layer, forming inter-gate dielectric and pattern the stack layers to form gate pattern.

Regarding claims 28-31, it is conventional to one having ordinary skill in the art that the silicon oxide layer is formed by thermally oxidizing and the conductive pattern is made of polysilicon, forming an upper conductive pattern (control gate) and a capping layer on the upper conductive layer.

Regarding claims 32-35, it is obvious to one having ordinary skill in the art that CVD is well known to be used to form buffer insulation layer and diffusion barrier layer of silicon nitride and it is obvious in the art that the thermal oxidation is performed for a lower edge of the floating gate in order to thermally oxidize the oxide layer below the floating gate and thermally oxidize the lower edge of floating gate to reduce ions leaking/short circuit.

If Applicants are aware of better art than that which has been cited, they are required to call such to attention of the examiner.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P. Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (7-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao P. Le
Examiner